IN THE CLAIMS:

Following is a complete listing of all claims in the application, with an indication of the status of each:

Claim 1 (Currently Amended)). A vertical field effect transistor including

a semiconductor pillar conduction channel,

gate electrodes in trenches adjacent said semiconductor pillar,

fig. 22C, 37C

a layer of insulator adjacent said gate electrodes and opposite said semiconductor pillar,

sidewalls adjacent said semiconductor pillar above said gate electrodes in said trenches,

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insulator material in said trenches above said gate electrodes and ~~adjacent~~ **between** said sidewalls **and said layer of insulator**, said insulator material being selectively etchable relative to said sidewalls and said semiconductor pillar.

Claim 2 (Currently Amended). A vertical transistor as recited in claim 1, further including isolation material adjacent said layer of insulator ~~and~~ surrounding said vertical transistor, said isolation material being selectively etchable relative to said layer of insulator.

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Claim 3 (Currently Amended). A vertical transistor as recited in claim 2, further including

a contact formed in an opening in said isolation material adjacent said **layer of** insulator to a conductive region at an end of said pillar.

not OK, should be insulator material [2020] fig. 22C

Claim 4 (Original). A vertical transistor as recited in claim 1, further including

a contact formed in an opening to an end of said pillar, and

a contact formed in an opening adjacent to and extending above said pillar to said gate structure and insulated from said pillar by an insulating sidewall on said pillar.

Claim 5 (Original). A vertical transistor as recited in claim 1, further including a spacer in said trench between said gate structure and a bottom of said trench.

Claim 6 (Previously Presented). An integrated circuit device including isolation material surrounding transistor locations in a substrate, vertical field effect transistors formed at said transistor locations and having a gate electrode structure formed in a trench, a layer of insulator material in said trench between said isolation material and said gate electrode structure, said isolation material being selectively etchable relative to said layer of insulator and a contact opening formed along an interface of said layer of insulator material and said isolation material.

Claim 7 (Original). A device as recited in claim 6, wherein said gate structure includes dual gate electrodes extending on opposite sides of a conduction channel.

Claim 8. (Currently Amended) A device as recited in claim 6, further including a contact formed in said contact opening in said isolation material adjacent said **layer of** insulator and extending to a conductive region extending below said pillar.

Same as claim 3

Claim 9 (Original). A device as recited in claim 6, further including a contact formed in an opening to an end of said pillar, and a contact formed in an opening adjacent to and extending above said pillar to said gate structure and insulated from said pillar by an insulating sidewall on said pillar.

Claim 10 (Currently Amended). A device as recited in claim ~~61~~ **6**, further including a spacer in said trench between said gate structure and a bottom of said trench.

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11 (Withdrawn). A method of making a semiconductor device including a field effect transistor, said method including steps of

forming a semiconductor pillar in a trench in a body of a first insulating material, said trench extending to a layer of semiconductor material,

forming a layer of a second insulating material on walls of said trench, and

etching a contact opening to said semiconductor material through said first insulating material selectively and adjacent to said second insulating material.

12 (Withdrawn). A method as recited in claim 11, including further steps of

forming a gate structure adjacent sides of said pillar,

forming layers and/or sidewalls of selectively etchable materials over said gate structure and said pillar, and

forming contact openings to an end of said pillar and said gate structure by selective etching of said layers at locations above and adjacent said pillar, respectively.

13 (Withdrawn). A method as recited in claim 11, including further steps of

defining a height of said pillar by thickness of a layer of sacrificial material.

14 (Withdrawn). A method as recited in claim 13, wherein said sacrificial material is germanium oxide.

15 (Withdrawn). A method as recited in claim 11, wherein said step of forming said pillar is performed by epitaxial semiconductor growth in a trench.

16 (Withdrawn). A method as recited in claim 11, wherein said step of forming said pillar is performed by etching of a layer of semiconductor material.

17 (Withdrawn). A method as recited in claim 11, including a further step of

limiting a dimension of said pillar by a distance between isolation structures.

Claim 18 (Original). A transistor comprising

a substrate,

fig. 36A-36C, 38A-38C

a first diffusion,

a second diffusion above said first diffusion,

a channel extending vertically between said first diffusion and said second diffusion,

a gate structure extending on at least one side of said channel, and

a contact to said first diffusion borderless to said gate structure.

Claim 19 (Original). A transistor as recited in claim 18, wherein said transistor is a vertical transistor and wherein said first diffusion is formed in said substrate and said second diffusion is formed on the channel.

Claim 20 (Previously Presented). A transistor as recited in claim 18, wherein said gate structure extends on two sides of said channel.

Claim 21 (Original). A transistor as recited in claim 19, wherein a contact to said gate extends above and on two sides of said second diffusion.

Claim 22 (Original). A transistor as recited in claim 19, further including separate contacts to separate portions of said gate structure on different sides of said channel.

Claim 23 (Original). A transistor as recited in claim 18, wherein said gate structure extends on at least three sides of said channel.

Claim 24 (Original). A transistor as recited in claim 18, further including a contact to said second diffusion borderless to said gate structure.

Claim 25 (Original). A transistor as recited in claim 18, wherein said transistor

comprises a pillar of single crystal silicon having an edge.

Claim 26 (Original). A transistor as recited in claim 25, wherein said pillar comprises said first diffusion, said channel and said second diffusion, said gate structure extending adjacent said pillar.

Claim 27 (Original). A transistor as recited in claim 26, wherein said first diffusion extends into single crystal silicon beneath said pillar and extends below said gate structure for formation of a contact adjacent said gate structure.

Claim 28 (Original). A transistor as recited in claim 26, further comprising an insulator adjacent said gate structure, wherein said contact to said first diffusion comprises a conductive layer adjacent said insulator.

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Claim 29 (Currently Amended). A transistor as recited in claim 26, wherein **a contact to** said gate structure is borderless to said second diffusion.

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Claim 30 (Currently Amended). A transistor as recited in claim 26, wherein said contact to said second diffusion ~~**comprises**~~ **extends adjacent to** a spacer **which is** self-aligned to said edge.

Claim 31 (Original) A transistor as recited in claim 26, wherein said pillar extends above said gate structure.

Claim 32 (Original). A transistor as recited in claim 18, further comprising an isolation structure, wherein said transistor is self-aligned to said isolation structure.

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Claim 33 (Currently Amended). A transistor as recited in claim 18, further

comprising

a contact between said first diffusion and another diffusion forming part of a second transistor, wherein said contact between said first diffusion and said another diffusion extends over **an area of** insulation between said first transistor and said second transistor.

Claim 34 (Original). A transistor as recited in claim 33, wherein said insulation comprises an etched-and-deposited isolation structure.

Claim 35 (Original). A transistor as recited in claim 34 wherein said substrate comprises SOI having buried oxide isolation and wherein said insulation comprises said buried oxide isolation.

Claim 36 (Original). A transistor as recited in claim 33, wherein said first transistor and said second transistor comprise an inverter and wherein said contact to said first diffusion is a contact to said inverter.

Claim 37 (Original). A transistor as recited in claim 18, wherein said gate structure comprises a continuous interior wall entirely surrounding said channel and spaced therefrom by a dielectric layer.

Claim 38 (Original). A transistor as recited in claim 18 wherein said gate structure is self-aligned to said channel.

Claim 39 (Original). A transistor as recited in claim 18 wherein said first diffusion comprises a dopant species provided separately from said second diffusion.

Claim 40 (Original). A transistor as recited in claim 18, wherein said channel is of sub-lithographic width.

Claim 41 (Original). A transistor as recited in claim 18, wherein said first diffusion includes

top and side surfaces covered by a dielectric material,

a borderless opening at least through a portion of the dielectric material on said top surface, and

a first diffusion contact formed in the opening.

Claim 42 (Original). A transistor as recited in claim 18, wherein said second diffusion includes

top and side surfaces covered by a dielectric material,

a borderless opening at least through a portion of the dielectric material on said top surface, and

a second diffusion contact formed in the opening.

Claim 43 (Original). A transistor as recited in claim 18, wherein said gate structure includes

top, bottom and side surfaces covered by a dielectric material,

a borderless opening at least through a portion of the dielectric material on said top surface, and

a gate contact formed in the opening.

Claim 44 (Original). A transistor as recited in claim 18, wherein said first diffusion, said second diffusion and said gate structure each include a borderless contact.